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APPLICATION NO.	FILING DATE	FIRST NAMED INVENTOR	ATTORNEY DOCKET NO.	CONFIRMATION NO.
09/966,316	09/27/2001	J. Daniel Mis	9180-5	5045
20792	7590	11/26/2003	EXAMINER	
MYERS BIGEL SIBLEY & SAJOVEC PO BOX 37428 RALEIGH, NC 27627			VESPERMAN, WILLIAM C	
			ART UNIT	PAPER NUMBER
			2813	

DATE MAILED: 11/26/2003

Please find below and/or attached an Office communication concerning this application or proceeding.

Office Action Summary

Application No.

09/966,316

Applicant(s)

MIS ET AL.

Examiner

William C. Vesperman

Art Unit

2813

NW

-- The MAILING DATE of this communication appears on the cover sheet with the correspond nc address --

Period for Reply

A SHORTENED STATUTORY PERIOD FOR REPLY IS SET TO EXPIRE 03 MONTH(S) FROM THE MAILING DATE OF THIS COMMUNICATION.

- Extensions of time may be available under the provisions of 37 CFR 1.136(a). In no event, however, may a reply be timely filed after SIX (6) MONTHS from the mailing date of this communication.
- If the period for reply specified above is less than thirty (30) days, a reply within the statutory minimum of thirty (30) days will be considered timely.
- If NO period for reply is specified above, the maximum statutory period will apply and will expire SIX (6) MONTHS from the mailing date of this communication.
- Failure to reply within the set or extended period for reply will, by statute, cause the application to become ABANDONED (35 U.S.C. § 133).
- Any reply received by the Office later than three months after the mailing date of this communication, even if timely filed, may reduce any earned patent term adjustment. See 37 CFR 1.704(b).

Status

- 1) ☒ Responsive to communication(s) filed on 10/22/03.
- 2a) ☒ This action is **FINAL**. 2b) ☐ This action is non-final.
- 3) ☐ Since this application is in condition for allowance except for formal matters, prosecution as to the merits is closed in accordance with the practice under *Ex parte Quayle*, 1935 C.D. 11, 453 O.G. 213.

Disposition of Claims

- 4) ☒ Claim(s) 1-28 and 62-81 is/are pending in the application.
- 4a) Of the above claim(s) _____ is/are withdrawn from consideration.
- 5) ☒ Claim(s) 17 - 28, 78 and 80 is/are allowed.
- 6) ☒ Claim(s) 1, 2, 13-15, 62, 66-69, 77, 79 and 81 is/are rejected.
- 7) ☒ Claim(s) 3 - 12, 16, 63 - 65 and 70 - 73 and 76 is/are objected to.
- 8) ☐ Claim(s) _____ are subject to restriction and/or election requirement.

Application Papers

- 9) ☐ The specification is objected to by the Examiner.
- 10) ☒ The drawing(s) filed on 27 September 2001 is/are: a) ☒ accepted or b) ☐ objected to by the Examiner.
Applicant may not request that any objection to the drawing(s) be held in abeyance. See 37 CFR 1.85(a).
Replacement drawing sheet(s) including the correction is required if the drawing(s) is objected to. See 37 CFR 1.121(d).
- 11) ☐ The oath or declaration is objected to by the Examiner. Note the attached Office Action or form PTO-152.

Priority under 35 U.S.C. §§ 119 and 120

- 12) ☐ Acknowledgment is made of a claim for foreign priority under 35 U.S.C. § 119(a)-(d) or (f).
a) ☐ All b) ☐ Some * c) ☐ None of:
1. ☐ Certified copies of the priority documents have been received.
2. ☐ Certified copies of the priority documents have been received in Application No. _____.
3. ☐ Copies of the certified copies of the priority documents have been received in this National Stage application from the International Bureau (PCT Rule 17.2(a)).
* See the attached detailed Office action for a list of the certified copies not received.
- 13) ☐ Acknowledgment is made of a claim for domestic priority under 35 U.S.C. § 119(e) (to a provisional application) since a specific reference was included in the first sentence of the specification or in an Application Data Sheet. 37 CFR 1.78.
a) ☐ The translation of the foreign language provisional application has been received.
- 14) ☐ Acknowledgment is made of a claim for domestic priority under 35 U.S.C. §§ 120 and/or 121 since a specific reference was included in the first sentence of the specification or in an Application Data Sheet. 37 CFR 1.78.

Attachment(s)

- 1) ☒ Notice of References Cited (PTO-892)
- 2) ☒ Notice of Draftsperson's Patent Drawing Review (PTO-948)
- 3) ☒ Information Disclosure Statement(s) (PTO-1449) Paper No(s) 9.
- 4) ☐ Interview Summary (PTO-413) Paper No(s). _____
- 5) ☐ Notice of Informal Patent Application (PTO-152)
- 6) ☐ Other: _____

DETAILED ACTION

1. This action is in response to applicant's amendment of October 22, 2003.

Claim Rejections - 35 USC § 103

2. The following is a quotation of 35 U.S.C. 103(a) which forms the basis for all obviousness rejections set forth in this Office action:

(a) A patent may not be obtained though the invention is not identically disclosed or described as set forth in section 102 of this title, if the differences between the subject matter sought to be patented and the prior art are such that the subject matter as a whole would have been obvious at the time the invention was made to a person having ordinary skill in the art to which said subject matter pertains. Patentability shall not be negated by the manner in which the invention was made.

3. Claims 1, 2, 13, 14, 15, 62, 66, 67, 68, 69, 77, 79 and 81 are rejected under 35 U.S.C. 103(a) as being unpatentable over Degani (EP 0 782 191 A2) in view of Sambucetti et al. (US 6,335,104).

Degani (EP 0 782 191 A2) teaches (Figure 1, column 4, lines 11 – 48) first and second input/output pads formed on of the substrate of chip 18, where the first input/output pads receive solder bumps (191 and 201) in order to connect to input/output pads formed on the substrate of chip 19 and second input/output pads (314 and 318) connecting to wire bonds (212 and 214) in order to connect to input/output pads on the substrates of chips 16 and 21 respectively.

Degani (EP 0 782 191 A2) does not teach providing first and second metallurgy structures on the respective first and second input pads having a shared metallurgy structure adapted to receive solder and wire bonds.

Sambucetti et al. (US 6,335,104) teaches (Figures 1 and 2, columns 5 – 7, lines 1 - 26) a method of preparing a copper bond pad (12) surface for electrical connection by

either a wirebond or a solder bump. Sambucetti et al. teaches forming a shared metallurgy structure (10) of the same composition and structure by depositing a diffusion barrier (16) comprising of nickel over and in contact with the copper bond pad (12) and a layer of gold (18) over and in contact with the nickel containing layer (16) for attaching a solder bump (40) or a wire bond (30).

Therefore, it would be obvious to one of ordinary skill in the art at the time of the invention to modify the method as taught by Degani to replace the first and second input/output pads for attaching solder bumps and wirebonds with shared metallurgy structures (10) comprising of a copper input/output pad (12), a nickel diffusion layer (16) over the copper input/output pad and a gold passivation layer (18) over the nickel diffusion layer (16) as taught by Sambucetti et al. for attaching a solder bump (40) or a wire bond (30), thereby simplifying the manufacturing process.

Additionally, Degani (EP 0 782 191 A2) teaches (Figures 1 and 2, columns 5 – 7, lines 1 - 26) that the first input/output pads of chip 18 receive solder bumps (191 and 201) in order to connect to input/output pads formed on the substrate of chip 19 and that the second input/output pads (314 and 318) of chip 18 are connected to wire bonds (212 and 214). When the chip 18 is bonded to chip 19 via the solder bumps as discussed, the wire bonds attached to chip 18 and the second substrate 19 are bonded to the first substrate 18 at the same time.

Allowable Subject Matter

4. Claims 17 – 28, 78 and 80 are allowed.

5. Claims 3 – 12, 16, 63 – 65 and 70 – 73 and 76 are objected to as being dependent upon a rejected base claim, but would be allowable if rewritten in independent form including all of the limitations of the base claim and any intervening claims.

The prior art does not teach or fairly suggest, in combination with the other claimed limitations, a method of providing metallurgy structures for input/output pads of an electronic device comprising of a substrate including semiconductor portions, and first and second input/output pads on the substrate, the method comprising: providing first and second metallurgy structures on the respective first and second input/output pads having a shared metallurgy structure comprising of underbump metallurgy layers on the respective input/output pads; barrier layers on the underbump metallurgy layers; and passivation layers on the barrier layers.

Conclusion

6. Applicant's submission of an information disclosure statement under 37 CFR 1.97(c) with the fee set forth in 37 CFR 1.17(p) on 6/30/2003 prompted the new ground(s) of rejection presented in this Office action. Accordingly, **THIS ACTION IS MADE FINAL**. See MPEP § 609(B)(2)(i). Applicant is reminded of the extension of time policy as set forth in 37 CFR 1.136(a).

A shortened statutory period for reply to this final action is set to expire **THREE MONTHS** from the mailing date of this action. In the event a first reply is filed within **TWO MONTHS** of the mailing date of this final action and the advisory action is not

mailed until after the end of the THREE-MONTH shortened statutory period, then the shortened statutory period will expire on the date the advisory action is mailed, and any extension fee pursuant to 37 CFR 1.136(a) will be calculated from the mailing date of the advisory action. In no event, however, will the statutory period for reply expire later than SIX MONTHS from the mailing date of this final action.

7. The prior art made of record and not relied upon is considered pertinent to applicant's disclosure.

Jao (US 6,415,974 B2) teaches a structure with solderbumps with improved coplanarity.

Chiang (US 2002/0086520) teaches a semiconductor device having a bump electrode.

Yung (US 5,162,257) teaches a solder bump fabrication method.

Ma (US 6,208,018 B1) teaches a piggyback multiple dice assembly.

Merrill et al. (US 5,886,393) teaches a bonding wire inductor for use in an integrated circuit.

Mis (5,902,686) teaches methods for forming an inter-metallic region between a solder bump and a under-bump metallurgy region.

Kuo (US 2002/0197842 A1) teaches a solder bump process using a solder reservoir.

Akram (US 2003/0143830 A1) teaches a multi-chip module with wirebonds and solder bumps attached.

Stlerman (US 2003/0107137 A1) teaches micro-mechanical device contact terminals for bonding wirebonds and solder bumps.

Elenius et al. (US 2001/0011764 A1) teaches chip scale package using large scale ductile solder balls.

Jiang et al. (US 2001/0020745 A1) teaches an interconnect component for a semiconductor die.

8. Any inquiry concerning this communication or earlier communications from the examiner should be directed to William C. Vesperman whose telephone number is 703-305-1939. The examiner can normally be reached on Mon. - Fri., 8:00 - 4:30.

If attempts to reach the examiner by telephone are unsuccessful, the examiner's supervisor, Carl Whitehead, Jr. can be reached on 703-308-4940. The fax phone numbers for the organization where this application or proceeding is assigned are 703-872-9318 for regular communications and 703-872-9319 for After Final communications.

Any inquiry of a general nature or relating to the status of this application or proceeding should be directed to the receptionist whose telephone number is 703-308-0956.


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Art Unit 2813

November 16, 2003


ERIK J. KIELIN
PRIMARY EXAMINER